IN THE SPECIFICATION

Please amend Paragraph 0019, Line 2 to read as follows:

[0019] Examples of a nonplanar transistor 400 in accordance with embodiments of present invention are illustrated in Figure 4A-4C. Nonplanar ~~transitor~~ transistor 400 is formed on an insulating substrate 402. In an embodiment of the present invention, insulating substrate 402 includes a lower monocrystalline silicon substrate 404 upon which is formed in insulating layer 406, such as a silicon dioxide film. Nonplanar transistor 400, however, can be formed on any well-known insulating substrate such as substrates formed from silicon dioxide, nitrides, oxides, and sapphires.

Please amend Paragraph 0037, Line 2 to read as follows:

[0037] Next, standard photolithography and etching techniques are used to define a semiconductor body or fin 620 in the semiconductor film 608 for the tri-gate ~~transister~~ transistor as shown in Figure 6B. In an embodiment of the present invention, the fin or body 620 is patterned to have a width 618 which is equal to or greater than the width desired of the gate length (Lg) of the fabricated transistor. In this way, the most stringent photolithography constraints used to fabricate the transistor are associated with the gate electrode patterning and not the semiconductor body or fin definition. In an embodiment of the present invention, the semiconductor body or fins will have a width 618 less than or equal to 30 nanometers and ideally less than or equal to 20 nanometers. In an embodiment of the present invention, the semiconductor bodies or fins have a width 618 approximately equal to the silicon body height 609. In an embodiment of the present invention, the fins or bodies 620 have a width 618 which is between ½ the semiconductor body height 609 and two times the semiconductor body height 609.

Please amend Paragraph 0039, Line 1 to read as follows:

[0039] The ~~semiconductor~~ semiconductor film 608 can be patterned into fins and landing pads by well known photolithography and etching techniques which generally include the formation of a photoresist mask by masking, exposing, and developing a blanket deposited photoresist film, and then etching semiconductor film in alignment with the photoresist mask to form one or more silicon bodies or fins 620 and source and drain landing pads 622 and 624 respectively. Semiconductor film 608 is etched until the underlying buried insulating layer 606 is exposed. Well-known semiconductor etching techniques, such as anisotropic plasma etching or reactive ion etching can be used to etch semiconductor film 608 in alignment with the photoresist mask. After semiconductor film 608 is etched to form a semiconductor body or fin 620 (and source/drain landing pads 622 and 624, if desired) the photoresist mask is removed by well-known techniques, such as by chemical stripping and O_2 ashing, to produce the substrate shown in Figure 6B.

Please amend Paragraph 0046, Line 2 to read as follows:

[0046] Next, source 640 and drain 642 regions for the transistor are formed in semiconductor body 620 on opposite sides of gate electrode 630 as shown in Figure 6G. Source and drain regions 640 and 642, respectively, can be formed by placing dopants 644 into semiconductor bodies 620 on both sides 639, 641 of gate electrode 630 in order to form regions 640 and 642 as shown in Figure 6G. If source and drain landing pads 622 and 624 are utilized, they are also doped at this time. For a PMOS tri-gate transistor, the semiconductor fin or body 620 on opposite sides of the gate electrode are doped to a p type conductivity and to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3 to form the source and drain regions. For a NMOS tri-gate transistor, the semiconductor fin or body 620 on opposite sides of the gate electrode

is doped with n type conductivity ions to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3 to form source and drain regions. In an embodiment of the present invention, the body is doped by ion-implantation. In an embodiment of the present invention, the ion-implantation occurs in a vertical direction (i.e., a direction perpendicular to substrate 600) as shown in Figure 6G. When gate electrode 630 is a polysilicon gate electrode, it can be doped during the ion-implantation process by first removing hard mask 634. A polysilicon gate electrode 630 will act as a mask to prevent the ion-implantation step from doping the channel region(s) 648 of the nonplanar transistor. The channel region 648 is the portion of the semiconductor body 620 located beneath or surrounded by the gate electrode 636. If gate electrode 636 is a metal electrode, the dielectric hard mask 634 can be used to block the doping during the ion-implantation process. In other embodiments, other methods, such as solid source diffusion, may be used to dope the semiconductor body to form source and drain extensions. At this point, fabrication of a nonplanar ~~transitor~~ transistor with a partially or fully wrapped around gate electrode is complete.

Please amend Paragraph 0047, Line 5 to read as follows:

[0047] In embodiments of the present invention, "halo" regions can be formed in silicon body prior to the formation of a source/drain regions or source/drain extension regions. Halo regions are doped regions formed in the channel region 648 of the device and are of the same conductivity but of a slightly higher concentration than the doping of the channel region of the device. Halo regions can be formed by ~~ion-implantating~~ ion-implanting dopants beneath the gate electrode by utilizing large angled ion-implantation techniques.

Please amend Paragraph 0061, Line 2 to read as follows:

[0061] Additionally, if desired, silicide 812, such as but not limited to cobalt silicide, nickel ~~silide~~ silicide, and titanium silicide may be formed onto the exposed surfaces of the semiconductor body or onto the additionally added silicon film as shown in Figure 8C. Silicide can be formed onto the top surface and side surfaces of the exposed semiconductor body or additional silicon by utilizing a self-aligned or "salicide" process. In a self-aligned or "salicide" process, a refractory metal film, such as but not limited to titanium, nickel and cobalt can be blanket deposited over the substrate including the silicon regions and dielectric regions. The substrate is then annealed to a temperature sufficient to cause the blanket deposited metal layer to react with the silicon containing regions to form a silicide. Regions, such as sidewalls spacers 808, as well as insulating layer 606 will not react with the metal and the metal will remain unreacted metal in these areas. Next, a selective wet etch can be used to remove the unreacted metal while leaving the metal silicide 812. In this way, silicide can be selectively formed only onto the silicon or semiconductor regions of a substrate as shown in Figure 8C.